**TSPi Plan Summary - Form SUMP**

***Note: Fields in green color can be found in the “SUMP\_Part2.pdf”. The process dashboard was not able to produce the information in marked with red color.***

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Name | Nisha | | | Date | | | | | | 05/02/09 | |
| Team | Gang of four (Group 4) | | | Instructor | | | | | | Mel | |
| Part/Level | LOC Code Counter | | | Cycle | | | | | | 2 | |
| **Product Size** | | | **Plan** | | | |  | **Actual** | | | |
| Requirements pages (SRS) | | |  | | | |  |  | | | |
| Other text pages | | |  | | | |  |  | | | |
| High-level design pages (SDS) | | |  | | | |  |  | | | |
| Detailed design lines | | |  | | | |  |  | | | |
| Base LOC (B) (measured) | | | 1102 | | | |  | 1021 | | | |
| Deleted LOC (D) | | | 100 | | | |  | 65 | | | |
|  | | | (Estimated) | | | |  | (Counted) | | | |
| Modified LOC (M) | | | 102 | | | |  | 94 | | | |
|  | | | (Estimated) | | | |  | (Counted) | | | |
| Added LOC (A) | | | 1000 | | | |  | 706 | | | |
|  | | | (N-M) | | | |  | (T-B+D-R) | | | |
| Reused LOC (R) | | | 500 | | | |  | 225 | | | |
|  | | | (Estimated) | | | |  | (Counted) | | | |
| Total New & Changed LOC (N) | | |  | | | |  |  | | | |
|  | | | (Estimated) | | | |  | (A+M) | | | |
| Total LOC (T) | | | 1102 | | | |  | 1021 | | | |
|  | | | (N+B-M-D+R) | | | |  | (Measured) | | | |
| Total New Reuse LOC | | | 600 | | | |  | 706 | | | |
| Estimated Object LOC (E) | | | >70% | | | |  |  | | | |
| Upper Prediction Interval (70%) | | | <70% | | | |  |  | | | |
| Lower Prediction Interval (70%) | | |  | | | |  |  | | | |
| **Time in Phase (hours)** | | **Plan** | | |  | **Actual** | | |  | | **Actual %** |
| Management and miscellaneous | |  | | |  |  | | |  | |  |
| Launch and strategy | |  | | |  |  | | |  | |  |
| Planning | |  | | |  |  | | |  | |  |
| Requirements | |  | | |  |  | | |  | |  |
| System test plan | |  | | |  |  | | |  | |  |
| Requirements inspection | |  | | |  |  | | |  | |  |
| High-level design | |  | | |  |  | | |  | |  |
| Integration test plan | |  | | |  |  | | |  | |  |
| High-level design inspection | |  | | |  |  | | |  | |  |
| Implementation planning | |  | | |  |  | | |  | |  |
| Detailed design | |  | | |  |  | | |  | |  |
| Detailed design review | |  | | |  |  | | |  | |  |
| Test development | |  | | |  |  | | |  | |  |
| Detailed design inspection | |  | | |  |  | | |  | |  |
| Code | |  | | |  |  | | |  | |  |
| Code review | |  | | |  |  | | |  | |  |
| Compile | |  | | |  |  | | |  | |  |
| Code inspection | |  | | |  |  | | |  | |  |
| Unit test | |  | | |  |  | | |  | |  |
| Build and integration | |  | | |  |  | | |  | |  |
| System test | |  | | |  |  | | |  | |  |
| Documentation | |  | | |  |  | | |  | |  |
| Postmortem | |  | | |  |  | | |  | |  |
| Total | |  | | |  |  | | |  | |  |
| Total Time UPI (70%) | |  | | |  |  | | |  | |  |
| Total Time LPI (70%) | |  | | |  |  | | |  | |  |

**TSPi Plan Summary - Form SUMP (continued)**

|  |  |  |  |
| --- | --- | --- | --- |
| Name |  | Date |  |
| Team |  | Instructor |  |
| Part/Level |  | Cycle |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Defects Injected** | **Plan** |  | **Actual** |  | **Actual %** |
| Strategy and Planning |  |  |  |  |  |
| Requirements |  |  |  |  |  |
| System test plan |  |  |  |  |  |
| Requirements inspection |  |  |  |  |  |
| High-level design |  |  |  |  |  |
| Integration test plan |  |  |  |  |  |
| High-level design inspection |  |  |  |  |  |
| Detailed design |  |  |  |  |  |
| Detailed design review |  |  |  |  |  |
| Test development |  |  |  |  |  |
| Detailed design inspection |  |  |  |  |  |
| Code |  |  |  |  |  |
| Code review |  |  |  |  |  |
| Compile |  |  |  |  |  |
| Code inspection |  |  |  |  |  |
| Unit Test |  |  |  |  |  |
| Build and integration |  |  |  |  |  |
| System test |  |  |  |  |  |
| Total Development |  |  |  |  |  |
| **Defects Removed** | **Plan** |  | **Actual** |  | **Actual %** |
| Strategy and Planning |  |  |  |  |  |
| Requirements |  |  |  |  |  |
| System test plan |  |  |  |  |  |
| Requirements inspection |  |  |  |  |  |
| High-level design |  |  |  |  |  |
| Integration test plan |  |  |  |  |  |
| High-level design inspection |  |  |  |  |  |
| Detailed design |  |  |  |  |  |
| Detailed design review |  |  |  |  |  |
| Test development |  |  |  |  |  |
| Detailed design inspection |  |  |  |  |  |
| Code |  |  |  |  |  |
| Code review |  |  |  |  |  |
| Compile |  |  |  |  |  |
| Code inspection |  |  |  |  |  |
| Unit Test |  |  |  |  |  |
| Build and integration |  |  |  |  |  |
| System test |  |  |  |  |  |
| Total Development |  |  |  |  |  |

**TSPi Plan Summary Instructions - Form SUMP**

|  |  |
| --- | --- |
| **Purpose** | * This form holds plan and actual data for program parts or assemblies. |
| **General** | * An assembly could be a system with multiple products, a product with multiple components, or a component with multiple modules. * A part could be a module, component, or product. * Note: the lowest-level parts or modules typically have no system-level data, such as requirements, high-level design, or system test. |
| **Using the TSPi Tool** | When using the TSPi tool, the plan values are automatically generated.   * The time and size data are computed from the TASK and SUMS forms. * The defect values are automatically generated during the quality planning process (SUMQ).   The actual values are also automatically generated by the TSPi tool.   * Time and size values come from the LOGT, TASK, and SUMS forms. * Defect data come from the LOGD forms.   When not using the TSPi tool, follow the instructions below. |
| **Header** | * Enter your name, date, team name, and instructor's name. * Name the part or assembly and its level. * Enter the cycle number. |
| **Columns** | * Plan: This column holds the part or assembly plan data. * Actual: For assemblies, this column holds the sum of the actual data for the parts of the assembly (at the lowest level, the modules). |
| **Product Size** | * For text and designs, enter only the new and changed size data. * For program parts or assemblies, enter all the indicated LOC data. * Obtain the data from the SUMS form. |
| **Time in Phase** | * Enter estimated and actual time by phase. * For parts, obtain these data from the TASK forms for those parts. * For assemblies, obtain the part-level time data from the totals on the SUMT form and the assembly-level data from the assembly-level TASK form. * For example, HLD time would come from the assembly TASK form while total part unit test time would come from the SUMT form. * Actual %: Enter the percent of the actual development time by phase. |
| **Defects Injected** | * Enter estimated and actual defects injected by phase. * Enter the defect estimates while producing the quality plan. * For parts, obtain actual data from the LOGD forms for those parts. * For assemblies, get part-level defect data from the totals of the SUMDI form and assembly-level data from the assembly LOGD form. * For example, HLD defects would come from the assembly LOGD form while the total part coding defects would come from the SUMDI form. * Actual %: Enter the percent of the actual defects injected by phase. |
| **Defects Removed** | * Enter estimated and actual defects removed by phase. * Enter the defect estimates while producing the quality plan. * For parts, obtain actaul data from the LOGD forms for those parts. * For assemblies, obtain part-level defect data from the totals of the SUMDR form and assembly-level data from the assembly LOGD form. * For example, HLD review defects would come from the assembly LOGD form while the total part code review defects would come from the SUMDR form. * Actual %: Enter the percent of the actual defects removed by phase. |